REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-21 in the application. In a previous amendment, the Applicants amended Claims 1-2, 5, 8-9, 12, 15-16 and 19. In the present response, the Applicants have not amended, canceled or added any claims. Accordingly, Claims 1-21 are currently pending in the application.

I. Rejection of Claims 1-21 under 35 U.S.C. §102

The Examiner has rejected Claims 1-21 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,421,774 to Henry, *et al.* The Applicants respectfully disagree since Henry does not teach identifying and tracking conditional instructions including: (1) generating tags and link pointers for instructions located in a conditional execution block and (2) causing the link pointers to move through conditional link pointer register sets, wherein each of the sets corresponds to a stage of a pipeline of the processor, as the instructions associated with the link pointers and located in the conditional execution block move through each of the corresponding stages as recited in independent Claims 1, 8 and 15.

Henry relates to the prediction of conditional branch instruction outcomes associated with a microprocessor having a pipeline architecture. (*See* column 1, lines 8-10.) Henry discloses a microprocessor 100 having a fetcher 101 that fetches instructions according to the contents of an instruction pointer (IP) 142. The microprocessor 100 also includes a branch predictor 103 that controls the selection of the contents to be loaded into the IP 142 based upon a prediction of whether a conditional branch instruction will be taken. (*See* column 6, line 53 to column 7, line 16.) The

branch instruction address is piped downed with the branch instruction through the various stages of the microprocessor pipeline via registers. (*See* column 7, lines 28-31.) The branch predictor 103 also indicates information relating to its static prediction of the outcome of a conditional branch. The static prediction information is stored in a static prediction register and is piped down with the conditional branch instruction through the various stages of the pipeline via static predictor registers. (*See* column 7, lines 44-53.)

The Examiner asserts that the instruction pointers of Henry disclose the link pointers that are generated for instructions located in a conditional execution block as recited in independent Claims 1, 8 and 15. (*See* Examiner's Action, page 3.) The instruction pointers, however, are not generated for instructions located in a conditional execution block but instead are target addresses that the fetcher 101 uses to fetch instructions. (*See* column 6, lines 62-64.) The Applicants do not find where Henry even discloses a conditional execution block or, more specifically, generating a link pointer for instructions that are in a conditional execution block. The instruction pointers, therefore, do not teach the link pointers that are generated for instructions located in a conditional execution block as recited in independent Claims 1, 8 and 15.

Additionally, even assuming that the instruction pointers are link pointers, the IPs (144, 146, 148 and 140) and the static prediction registers (134, 136, 138 and 130) are not conditional link pointer register **sets** as asserted by the Examiner. (*See* Examiner's Action, pages 2-3.) Instead, each of the IPs is a **single register** wherein a branch instruction address is piped downed and each of the static prediction registers is a **single register** wherein static prediction information is piped down. Thus, instead of being a register set that link pointers move through, the IPs and the static prediction

registers are separate, single registers that have an instruction address or a static prediction information moving there through, respectively. Accordingly, Henry also does not teach conditional link pointer register sets, wherein each of the sets corresponds to a stage of a pipeline of a processor and link pointers move there through as instructions associated with the link pointers and located in the conditional execution block move through each of the corresponding stages as recited in independent Claims 1, 8 and 15.

Therefore, at least for the above reasons, Henry does not disclose each and every element of independent Claims 1, 8 and 15. As such, Henry does not anticipate Claims 1, 8 and 15 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to Claims 1-21 and allow issuance thereof.

II. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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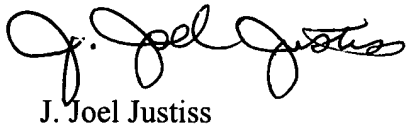

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